Qualification Results Summary of 24-LGA_CAV Package at STATS ChipPAC Korea

QUALIFICATION PLAN / STATUS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	**3 x 77**	**Pass**
Temperature Humidity Bias (THB)*	JEDEC *JESD22-A101*	**3 x 77**	**Pass**
Temperature Humidity Dwell (THD)*	JEDEC *JESD22-A101*	**3 x 77**	**Pass**
High Temperature Storage Life (HTSL)	JEDEC *JESD22-A103*	**1 x 45**	**Pass**
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	**3 x 11**	**Pass**
Latch-Up	JEDEC *JESD78*	**3/stress**	**Pass +/- 200mA**
Electrostatic Discharge *Human Body Model*	ESDA/JEDEC *JS-001*	**3/voltage**	**Pass +/-3000V**
Electrostatic Discharge *Field-Induced Charged Device Model*	ESDA/JEDEC *JS-002*	**3/voltage**	**Pass +/-1250V**

* These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 2 hours at 125ºC; 2. Soak – unbiased soak for 192 hours at 30ºC, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260ºC.